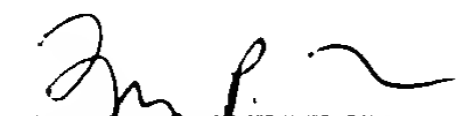Remarks:

The preliminary amendment is being filed in an effort to present an application in proper U.S. format and to present claims in proper U.S. claim idiom for examination.

The newly entered claims are fully supported in the original claims and in the claims of the German priority application. Replacement Figs. 2 and 3 have been provided in which labels have been added to the shown blocks.

An early action on the merits of the claims is requested.

Respectfully submitted,   Mark P. Weichselbaum
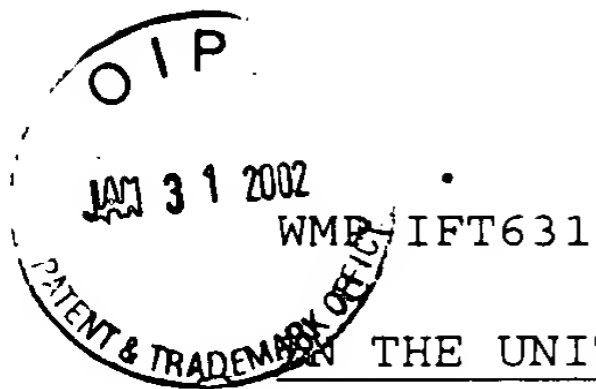   Reg. No. 43,248

For Applicant

MPW:cgm

January 15, 2002

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Rainald Sander

Applic. No. : 09/943,589

Filed : August 30, 2001

Title : Circuit Arrangement to Determine the Current in a Load Transistor

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Translated Specification:

Page 1, line 3, [Description].

Page 1, lines 5-6, [Circuit arrangement for detecting the current in a load transistor]

CIRCUIT CONFIGURATION FOR DETECTING THE CURRENT IN A LOAD

TRANSISTOR

Page 1, lines 8-11, [The present invention relates to a circuit arrangement having a load transistor and a current sensing transistor coupled to the load transistor in accordance with the features of the preamble of patent claim 1.] The present invention relates to a circuit arrangement having a load transistor and a current sensing transistor coupled to the load transistor.

Page 3, lines 11-12, [This aim is achieved by means of a circuit arrangement in accordance with the features of patent claim 1.]

Page 3, lines 14-15, [The subclaims relate to advantageous refinements of the invention.]

Page 5, lines 8-9, [The present invention is explained in more detail below using exemplary embodiments with reference to figures, in which:]

Page 13, line 1, [Patent Claims] I Claim:

Page 17, line 1, [Abstract] Abstract of the Disclosure:

Page 17, line, 12, [Figure 2]

Page 18, [List of reference symbols

Vdd	Supply potential
IN	Input terminal
D	Drain terminal
G	Gate terminal
S	Source terminal

UDS1, UDS2	Drain-source voltage
Uref	Reference voltage
K1	Comparator
P11, 21, P12	Terminal pins
BD	Bonding wire
Z_L	Load
BL1, BL2	Evaluation circuits
IC1, IC2	Integrated circuits
Us1	First current signal
Rs	Current sensing resistor
K2	Comparator
T2	Transistor
S1a, S1b	Transistors
R1, R2	Resistors
T4	Resistor
Us2	Second current signal]